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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/627,855	07/25/2003	Min-su Kim	SAM-0436	2651

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EXAMINER	
COX, CASSANDRA F	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 01/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/627,855	KIM, MIN-SU	
	Examiner	Art Unit	
	Cassandra Cox	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-56* is/are pending in the application.

4a) Of the above claim(s) *43-45 and 49-51* is/are withdrawn from consideration.

5)☒ Claim(s) *1-14,27-42,46-48 and 52-56* is/are allowed.

6)☒ Claim(s) *15,16,21 and 22* is/are rejected.

7)☒ Claim(s) *17-20 and 23-26* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 15-16 and 21-22 are rejected under 35 U.S.C. 102(e) as being anticipated by Jia et al. (U.S. Patent No 6,633,188).

In reference to claim 15 Jia discloses in Figure 3 a sense amplifier comprising: a first sense-amplifying unit (250, 252, 256, 270, 278), which sense-amplifies an input signal (D) in response to a clock signal (CLK) and a reset signal (Clear) and generates an output signal (/S); a second sense-amplifying unit (260, 262, 266, 272, 276), which sense-amplifies a complementary signal (inverted version of input D output from inverter 280) of the input signal (D) in response to the clock signal (CLK) and the reset signal (Clear) and generates a complementary signal (/R) of the output signal; a controller (254, 274) which is connected to the first sense-amplifying unit (250, 252, 256, 270, 278) and the second sense-amplifying unit (260, 262, 266, 272, 276), sets the output signal (/S) and resets the complementary output signal (/R) of the output signal in response to the reset signal (Clear) and an inverted signal (/Clear) of the reset signal; and a current source (282) which is connected to the first sense-amplifying unit (250,

252, 256, 270, 278), the second sense-amplifying unit (260, 262, 266, 272, 276), and the controller (254, 274) and responds to the clock signal (CLK). The same applies to claim 21 wherein the set and reset states are seen to be reversed.

In reference to claim 16, Jia discloses in Figure 3 the circuit further comprising a first inverting buffer (206), which buffers and inverts the output signal (/S); and a second inverting buffer (208), which buffers and inverts the complementary signal (/R) of the output signal. The same applies to claim 22.

Allowable Subject Matter

3. Claims 1-14, 27-42, 46-48, and 52-56 are allowed.

4. Claims 17-20 and 23-26 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

5. The following is a statement of reasons for the indication of allowable subject matter: Claims 17 and 23 would be allowable because the closest prior art of record fails to disclose a circuit as shown in Figure 4 wherein the first sense-amplifying unit (31) comprises a first PMOS transistor (P311); a second PMOS transistor (P312); a third PMOS transistor (P313); a first NMOS transistor (N311); a second NMOS transistor (N312); and a third NMOS transistor (N313) having the required connections as called for in the claims in combination with the rest of the limitations of the base claims and any intervening claims. Claims 18 and 24 would be allowable because the closest prior art of record fails to disclose a circuit as shown in Figure 4 wherein the second sense-amplifying unit (33) comprises a first PMOS transistor (P331); a second

PMOS transistor (P332); a third PMOS transistor (P333); a first NMOS transistor (N331); a second NMOS transistor (N332); and a third NMOS transistor (N333) having the required connections as called for in the claims in combination with the rest of the limitations of the base claims and any intervening claims. Claims 19 and 25 would be allowable because the closest prior art of record fails to disclose a circuit as shown in Figure 4 wherein the controller comprises a first NMOS transistor (N451), a second NMOS transistor (N452), and a third NMOS transistor (N453) having the required connections as called for in the claims in combination with the rest of the limitations of the base claims and any intervening claims. Claims 20 and 26 would be allowable because the closest prior art of record fails to disclose a circuit as shown in Figure 2 wherein the current source (19) includes an NMOS transistor, wherein the drain of the NMOS transistor is commonly connected to the first sense-amplifying unit (11), the second sense-amplifying unit (13), and the controller (25), and the clock signal (CLK) is applied to the gate of the NMOS transistor, and the ground voltage is applied to the source of the NMOS transistor in combination with the rest of the limitations of the base claims and any intervening claims.

6. The following is an examiner's statement of reasons for allowance: Claims 1-14 are allowed because the closest prior art of record fails to disclose a circuit as shown in Figure 1 wherein the sense amplifier comprises a first controller (15) which is connected to the first sense-amplifying unit (11) and sets the output signal (O1) in response to a reset signal (RESET) and an inverted signal (/RESET) of the reset signal; a second controller (17) which is connected to the second sense-amplifying unit (13) and resets

the complementary signal (O2) of the output signal in response to the reset signal (RESET) and the inverted signal (/RESET) of the reset signal; and a current source (19) which is connected to the first sense-amplifying unit (11), the second sense-amplifying unit (13), the first controller (15), and the second controller (17) and responds to the clock signal in combination with the rest of the limitations of the base claims and any intervening claims. Claims 27-40 are allowed because the closest prior art of record fails to disclose a circuit as shown in Figure 3 wherein the sense amplifier comprises a first controller (35) which is connected to the first sense-amplifying unit (31) and sets the output signal (O1) in response to a reset signal (RESET) and an inverted signal (/RESET) of the reset signal; and a second controller (37) which is connected to the second sense-amplifying unit (33) and resets the complementary signal (O2) of the output signal in response to the reset signal (RESET) and the inverted signal (/RESET) of the reset signal in combination with the rest of the limitations of the base claims and any intervening claims. Claims 41-42, 46-48, and 52 are allowed because the closest prior art of record fails to disclose a circuit as shown in Figure 4 wherein the first sense-amplifying unit (31) comprises a first PMOS transistor (P311); a second PMOS transistor (P312); a third PMOS transistor (P313); a first NMOS transistor (N311); a second NMOS transistor (N312); and a third NMOS transistor (N313) having the required connections as called for in the claims in combination with the rest of the limitations of the base claims and any intervening claims. Claims 53 and 55 are allowed because the closest prior art of record fails to disclose a circuit as shown in Figure 4 wherein the second sense-amplifying unit (33) comprises a first PMOS transistor

(P331); a second PMOS transistor (P332); a third PMOS transistor (P333); a first NMOS transistor (N331); a second NMOS transistor (N332); and a third NMOS transistor (N333) having the required connections as called for in the claims in combination with the rest of the limitations of the base claims and any intervening claims. Claims 54 and 56 are allowed because the closest prior art of record fails to disclose a circuit as shown in Figure 4 wherein the controller comprises a first NMOS transistor (N451), a second NMOS transistor (N452), and a third NMOS transistor (N453) having the required connections as called for in the claims in combination with the rest of the limitations of the base claims and any intervening claims.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cassandra Cox whose telephone number is 571-272-1741. The examiner can normally be reached on Monday-Thursday from 7:00 AM to 4:30 PM and on alternate Fridays from 7:00 AM to 3:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CC

01/04/05

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